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Design of Low Power Compact Phase Locked Loop Circuit for Clocking Applications

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Abstract

The phase-locked loop is a technique that has contributed significantly to technology. advancements in many applications in the fast-evolving digital era. In this paper, a Phase Locked Loop (PLL) is designed using a 65nm CMOS technology node with a 1.2 V supply voltage. It features a PLL design with a minimum power consumption of 194.26 µW with better transient and DC responses in an analog-to-digital environment. The proposed PLL design provides good solution for many applications where a PLL is required with high performance but must be accommodated in less area and low power consumption than state-of-the-art methods. This PLL not only works at high speed but also makes the whole system work at low power in a very effective manner, which suits the present digital electronics circuits Analysis and simulation of on-chip PLL-based clocking generator circuits for high-speed serial link applications. An overview of high-speed links, along with the basic building blocks that make up a serial link, is presented. The fundamentals of PLLs are introduced and a complete guide to the analysis and simulation of a charge-pump phase-locked loop-based clocking circuit at both behavioral as well as transistor levels is presented for use as a synthesizer in a serial link. Finally, a survey of potential future research areas to explore for both.PLLs in high-speed links as well as the complete serial link provided. an emphasis on signal integrity applications for future students' Graduate studies in the fields of Signal Integrity and Mixed-Signal IC Design.

Keywords: (PLL); Phase Frequency Detector/Charge Pump (PFD/CP); Low Pass Filter (LPF) Voltage-Controlled Oscillator (LCVCO); Analog Digital Environment (ADE)

1) Introduction:

The current era is all about compact battery devices used in electronic devices. A PLL is used in all SO de-vices where circuitry generates a system clock signal. A PLL has a feedback loop that controls the phase of the output signal with the input signal along with phase error. Figure 1 shows the block diagram of a PLL. It mainly consists of four blocks, namely a Phase. Frequency Detector (PFD), a Charge Pump with Low Pass Filter, a Voltage-Controlled Oscillator (VCO) to provide oscillations, and a frequency divider [1].

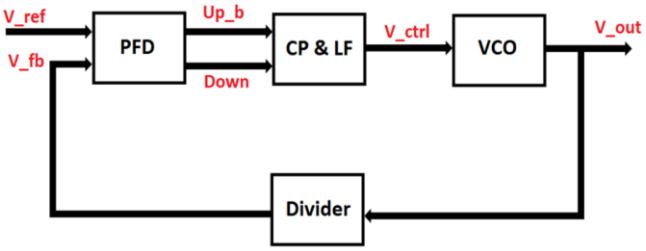

Figure 1. Block diagram of PLL [1].

2. Background

The most important metrics of a PLL are Order, Type, Hold-In range, lock-in range, and Pull-in range. The order of a PLL is determined by the number of poles in the loop while the type is determined by the number of integrators [9]. The VCO always has a pre-existing pole because it generates frequency from phase via an integration; thus, every PLL is at least of order 1 and type 1. As the loop-filter poles increase the PLL order and type increase as well. [10]. and the higher the type, the better the PLL is at tracking both frequency and phase. For instance, a type 2 PLL is capable of tracking both step changes in phase as well as frequency with zero steady-state phase error while a type 1 PLL can only track a step change in phase [9]. The hold-in range of a PLL is a measure of the DC loop gain and the range. of frequencies under which the PLL can maintain a lock. Lock-In range is. a measure of the range of frequencies under which a PLL can acquire lock. without slipping any clock cycles [10]. Finally, the Pull-In range is the measure. of the range of frequencies for which the PLL can acquire the lock by missing a few clock cycles. It is important to note that the hold-in range is the largest. Of the three the lock-in range is the smallest of the three metrics [2].

3. Related Work

Simple Link Design The generalized model of a High-Speed Serial Link (HSSL), as shown in Figure 2 [1]., consists of a serializer and transmitter (TX) driven by a PLL clock synthesizer.

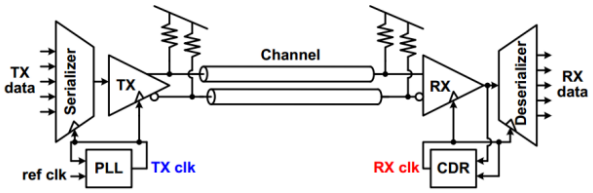

Figure 2: Typical High-Speed Link Block Diagram [2]

4. PLL Applications

Phase-locked loops (PLLs) are one of the most fundamental and ubiquitous. circuits found in any communications (wireless, wireline) and high-speed digital systems. Monolithic CMOS implementation of PLLs has gained lots of popularity over the last few decades due to an insatiable demand for high-performance digital systems. The most common uses of a PLL are in the form of frequency synthesizers and carrier/clock recovery circuits both in the RF domain as well as the high-speed digital domain [1].

5. Methodology

Previously, a multiplier was used as an analog phase detector, but it had a limited blocking range with a phase error of more than 90◦ where the output voltage is reduced. A digital phase detector was implemented where the mean value is proportional to the phase error [2]. The X-OR gate was used as a phase detector, which is linear, but if it were in phase and the error was greater than 180◦, it would lose its linearity [3]. Consequently, the phase-frequency detectors are designed to detect phase and frequency differences, which increases the speed of PLL. For the LPF design, a first-order filter could be used, but it would introduce ripples as the control voltage jumps high when current is injected from the charge pump. To solve this problem, a second-order low-pass filter was designed to suppress the generated ripple. Firstly, VCOs (Voltage Controlled Oscillators) were designed using LC oscillators or ring oscillators [3]. However, ring oscillators are not stable as they let the switching characteristics of logic gates fluctuate by +/−20% and the disadvantage of LC oscillators is that they have more matrix area. Therefore, the current starved VCO is realized in our proposed design. The PLL works in three states: Free Running state, Capture state, and Phase Lock state. As the name suggests, the free-running state refers to the phase in which no input voltage is

present. As soon as the input frequency is applied, the VCO starts switching and starts producing an output frequency to be compared, and this stage is called the capture state [4].

The frequency comparison stops as soon as the output frequency equals the input frequency. This phase is known as the phase-locked state. PLL is a convenient circuit block widely used in wireless applications and electronics, from cell phones to radios, televisions, Wi-Fi routers, areas like FM demodulators, AM demodulators, frequency synthesizers, and more recovery, etc. [5].

6. Design and Implementation

The proposed design of 65nm PLL was composed using cadence virtuoso and consisted of all the blocks of a Basic PLL. In this design, the number of transistors is reduced when compared to the existing designs [6]. Due to this, the area is reduced. The reduced transistors also lead to a decreased usage of power consumption and cost. The design of the blocks of the proposed PLL are shown and discussed below. It is obvious from the closed loop transfer function that the PLL is a low-pass filter. The PLL closed loop transfer function determines the bandwidth and thus the settling of the loop. Larger bandwidth leads to faster tracking but at the expense of larger loop gain and more noise appearing at the output due to the reference voltage.

I. Phase Frequency Detector

If the reference signal is faster by having its rising edge before the feedback signal, the Phase Frequency Detector (PFD) will give 1 in the "up signal" so that feedback (FB) frequency will be increased by the VCO. On the other hand, if the rising edge of FB comes first, this means the feedback signal is faster and the down signal is triggered to slow it down. Moreover, the up signal would give 1 instead of the shown -ve 1 in Fig.1.

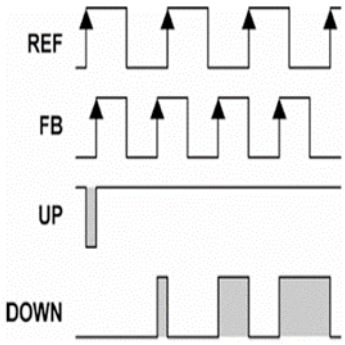

Figure 1: Basic operation of PFD. [2]

The Phase Frequency Detector (PFD) mainly consists of two D-flip flops and NAND gates. The block diagram of the PFD is shown below in Figure 2. The main purpose of a PFD is to compare the phase and frequency of the input signal with the feedback signal. It has two output signals, UP and DOWN [7]. The design of the low power edge triggered D-Flip flop with 1.2 V is designed with a reduced number of transistors, and the respective output waveforms are shown in Figure 2. This D flipflop has been used in designing the PFD [8]. Figure 3 shows PFD with two input signals, the reference signal CLKREF and the feedback signal, which is the output of VCO, CLKVCO each as an input to the two D-flipflops as shown below in Figure 3. The output of the first D-flipflop enables the positive current source and the negative current source of the charge pump. Assuming UP=DOWN=0, when CLKREF is high, UP rises thereby CLKVCO rises. When DOWN also is high, the NAND gate resets both the D-flipflops. UP and DOWN are high at the same time for a short while, at this point, the difference between their average values gives us the phase or frequency difference between both the input signals [9].

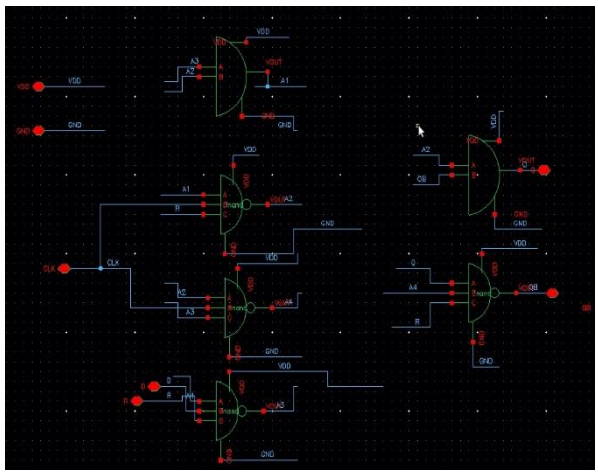

Figure 3. Schematic of D flip-flop

The modern phase detector used nowadays is the phase frequency detector (PFD) which is always accompanied by a charge pump (CP). The PFD converts the phase error at its input to a voltage that is converted by the CP to a correction current. PFD is much better in dealing with a large error in frequency than classical approaches as it has a linear range of radians.

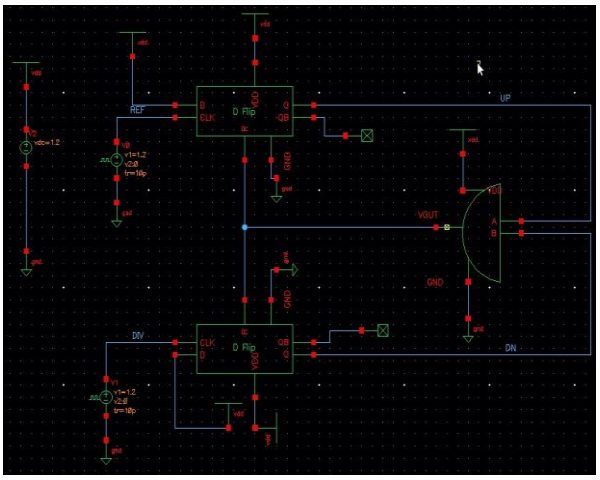

Figure 4. Schematic of Phase frequency detector

II. Charge Pump and Low Pass Filter

If the reference Charge pump generates I out in response to up and down signals generated from PFD. This I out will be used to charge and discharge the storage capacitor in the loop filter (LF). Hence, this would generate the voltage control signal for the VCO [5]. Hence, the behavioral model of CHP should give -I out for the input down signal and +I out for the input up signal. The value of I out is a parameter that is set to default value $10\mu A$ to target a low-power design as described in PLL design A multiplier factor of -1 or +1 is set and calculated by the Imult analog function [10]. Using a function enhances the readability of the code instead of repeating the same part of the code inside each event. If the value of the up signal is larger than the transition voltage (Vdd/2), then the up signal is detected. Likewise, if the value of the down signal is larger than the transition voltage, then the down signal is detected. When detecting the up signal only the multiplier factor will be 1 to charge the cap and hence increase the VCO control voltage [5]. On the other hand, if only the down signal is detected, this would set the multiplier to -1 to discharge the cap and therefore decrease the VCO control voltage [5]. The I out signal is written inside the events which are at any edge for up and down signals. I(out) am set to a -ve transition because -ve current means it flows out from the CHP and going to charge caps in the LF. Using +ve I(out) means the current enters the CHP which means caps are discharging Equation (1):

$$IPDI = KPDI \times \Delta \quad (1)$$

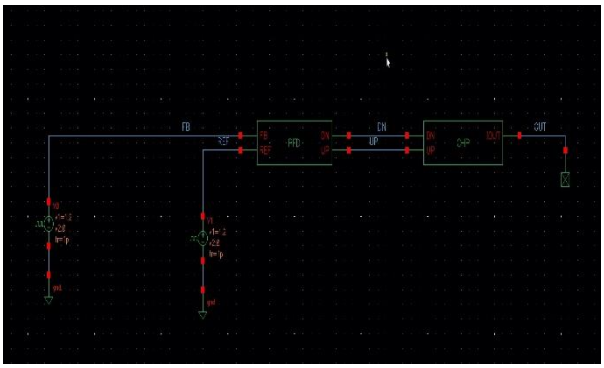

Figure 5. Test bench of the charge pump

The Low Pass Filter converts the charge pump current into voltage and the frequency of the VCO depends on the output of the LPF. When the charge pump current is positive, the oscillation frequency increases, otherwise it decreases [10]. Figure 4 shows the implementation of the Charge Pump along with the Low Pass Filter. The Low Pass Filter here is important because it filters out higher frequencies and influences the speed of the circuit [12].

III. Voltage Controlled Oscillator

Oscillators hold a pivotal role in the realm of analog design, particularly in the context of (PLL) circuits. PLLs rely on oscillators as key components for generating stable reference frequencies and achieving precise frequency synthesis and synchronization. In PLL designs, oscillators act as the reference signal source, providing a stable frequency against which other signals are compared and adjusted. This reference frequency is crucial for maintaining synchronization and phase alignment in applications. [10]. such as clock recovery, frequency modulation, and phase modulation [10]. The schematic of LCVCO is shown in Figure 6.

Steps for design LC oscillator

1. Select a power budget, P, and an output voltage swing, V0; the latter is preferably chosen not to drive the cross-coupled transistors into the triode region. From P and V0, determine ISS and Rp.
2. Find the smallest inductance that yields the necessary value of Rp at f0. This choice translates to the highest Q for the inductor.
3. Choose the necessary width of the cross-coupled transistors to allow complete switching of the tail current with a voltage swing of V0. In practice, we double or triple this width to ensure abrupt switching, nearly square-wave drain currents,

and hence a single-ended peak-to-peak swing close to (4/π) *ISS*Rp.

4. Add enough capacitance to the tank to obtain the highest desired frequency.
5. Implement ISS with a current mirror and minimize its noise contribution by proper sizing and filtering.

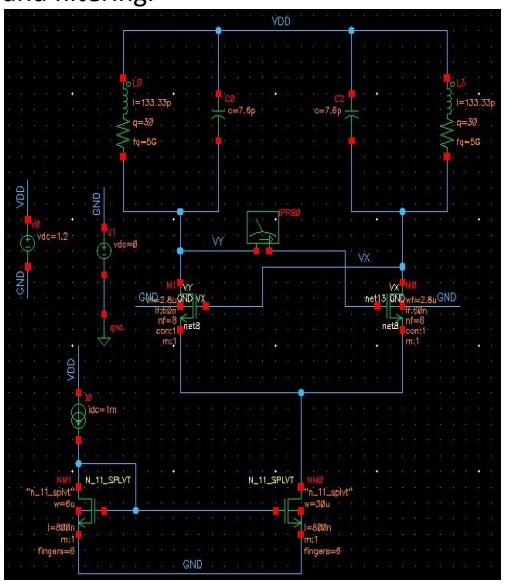

Figure 6. Schematic of Voltage controlled oscillator.

A VCO is a circuit that generates a periodic output whose frequency is a linear function of a control voltage [12]. The free-running frequency of the VCO can be called the open-loop frequency. In other words, the control voltage creates a frequency change relative to ωFR. The VCO gain may be either positive or negative, its polarity should affect the design of the phase detector. It is said that the oscillator is working in the current-limited regime when the tank amplitude increases with the increase in the bias current. oscillators within PLLs help regulate the output frequency by comparing it with a feedback signal and adjusting it accordingly. This feedback loop ensures that the output frequency remains locked to the desired reference frequency, enabling accurate frequency multiplication. For a VCO, a key figure of merit is the control voltage tuning range. Thus, we must perform a parametric analysis to observe the change in 'frequency' as well as KV CO as a function of 'Vctrl' Figure 7 shows transient analysis with output swing 0.8V.-using the calculator to determine the power and voltage swing using the expression shown in Fig.8 and Fig.9. Frequency simulation plots = 5GHZ, The result of phase noise at 1MHZ The output waveform for the simulated phase noise will look like Figure 8. In our case, we find that phase noise at a 1MHz offset is equal to -135.495dBc/Hz, which is very reasonable for LC VCO topology.

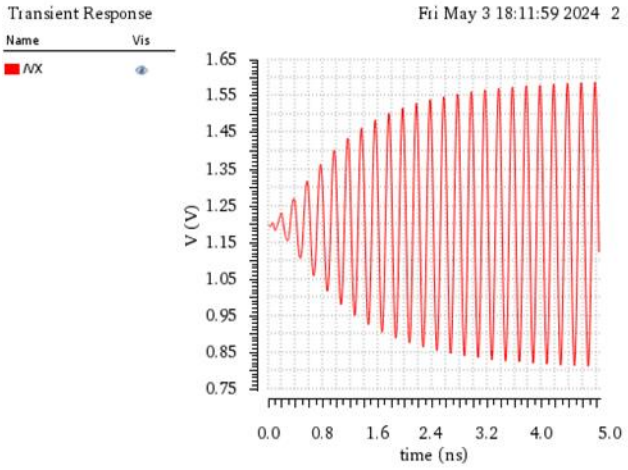

Figure 7: Vx output from the transient analysis.

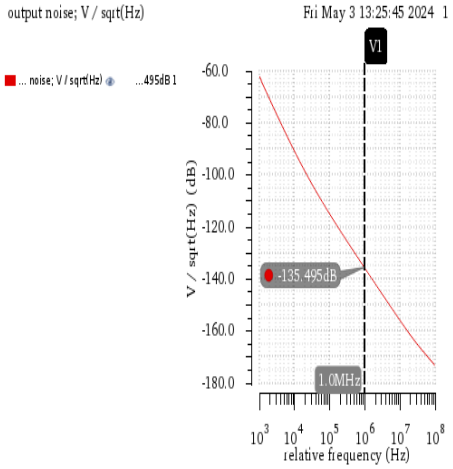

Figure 8. VCO Phase-Noise Simulation Plot

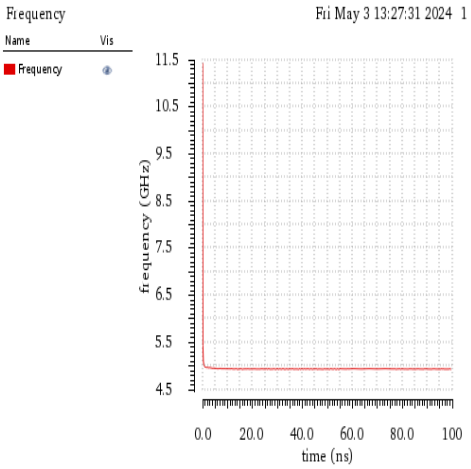

Figure 9. Frequency Simulation Plots

IV. Loop Filter

The loop filter is placed just after the charge pump to convert the current of the charge pump to a voltage that controls the VCO. It is being charged and discharged such that the control voltage of the VCO is formed from the average current of the charge pump. If no loop filter is present, the PLL is said to be of first order. As the order of the loop filter increases, the PLL order increases which makes the closed loop transfer function sharper, which is always the target of any designer, but this comes at the expense of the loop filter complexity.

V. Loop Filter Parameters

-loop filter parameters will be calculated from the equation

$\tau p = \sec(\phi m) - \tan(\phi m) / \omega u$ (1)

$\tau z = 1/wu\text{^}2 * \tau p$ (2)

the value of Rz = 31.415 Ω, Cz = 5.731p F, Cp = 180f f

VI. Divider

A frequency divider is needed to produce a clock signal that runs many times. faster than the reference clock. The PFD input clock and reference clock must be synchronized for the PLL to be in locked condition. To perform this task, we use a fractional-N divider circuit, which divides the VCO clock. by the highest power of 2 factors to synchronize the reference clock signal and the divider output clock [10]. The output of the VCO is provided to the PFD via the frequency divider circuit. as shown below in Figure 10,11. The frequency of the VCO output signal is divided in two by this frequency divider block.

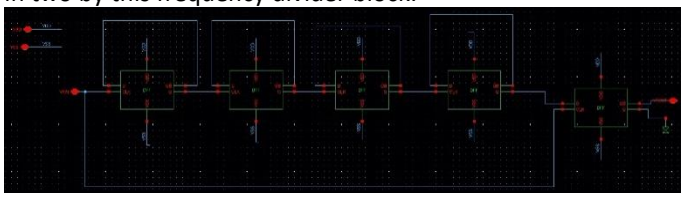

Figure 10. Schematic of the frequency divider

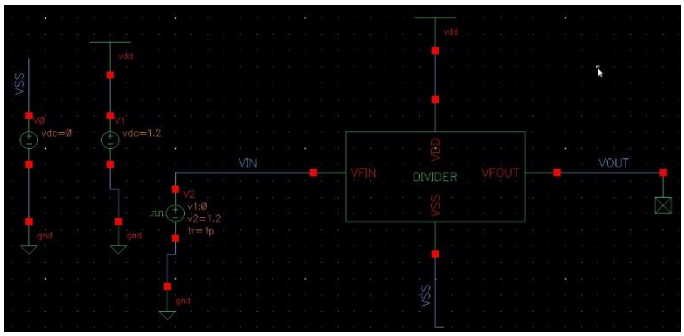

Figure 11. Test Bench the frequency divider.

The main functionality of the frequency divider is to change the divide ratio so the output frequency of the VCO can change from one channel to another. This is achieved by implementing a programmable divider. In the case of integer-N frequency synthesizers, Fout = N x F(ref) which indicates that the VCO output is divided by an integer, the most popular technique used as a frequency divider is a pulse swallow frequency divider [10].

6. Simulations Result and Discussion.

Figure 12 shows the total architecture of the behavioral model. The PLL achieves lock within the first 100ns because in the testbench provides an initial condition of Vctrl = 0.6V and keeps the current at the loop-filter capacitors at an initial condition of 0A. These initial conditions are provided to ensure that the simulation time is small.

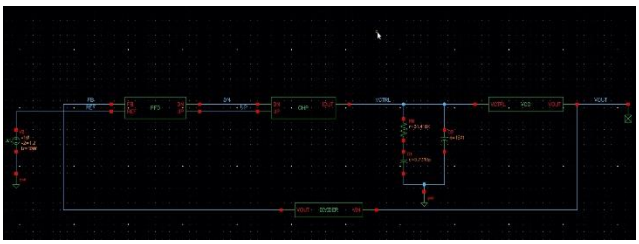

Figure 12. The architecture of Proposed PLL

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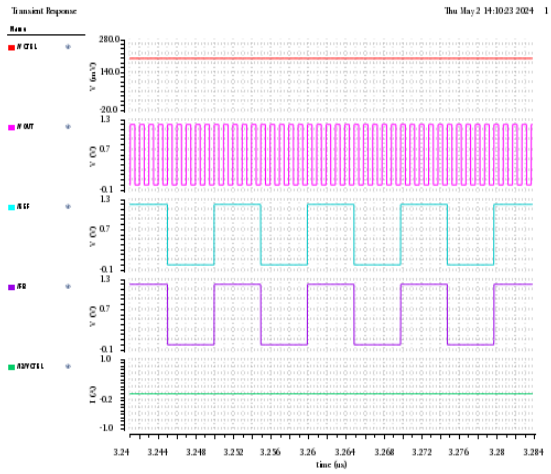

Figure 13. Transient and DC analysis of proposed PLL

Here, in Figure 11 the use of a novel design for PFD and a charge pump is used for reducing the power usage of the whole system and it also shows how they are incorporated in the entire PLL. Figure 13 shows transient and DC analysis of the proposed PLL that verifies the working of the PLL effectively. This not only shows the output PFD, i.e., UP and DOWN signals that act according to the clock signal but also shows the output waveforms of the charge pump which vary according to the input signals. When both the input signals i.e., REF and feedback are high, the output of the charge pump is high; when both the input signals are low, there is a drop in the output signal of the charge pump, which is given as input to the VCO.

Figure 13 shows the two input signals to the Charge Pump, UP and DOWN signals red and green respectively which are observed to be inverse of each other. The output signal of Charge Pump is purple as an OUT signal which is given as the input to the VCO as a control signal. The design of a PLL is done in cadence virtuoso tool by an Analog design environment using a 65nm node. Here, the transient and DC analysis of the proposed PLL and its blocks are discussed. A reference signal and a clock feedback signal are given as input to the PFD with output as UP and DOWN Signals. as shown below in Figure 14. The output of the charge pump is given to the VCO, which acts as a Voltage control signal, and the output of the VCO is given to a Frequency Divider where the output frequency is N/2, which is the feedback signal given back to the PFD. If the reference Charge pump generates Iout in response to up and down signals generated from PFD this Iout will be used to charge and discharge of the storage capacitor in the loop filter (LF) Hence, this would generate the voltage control signal for the VCO.

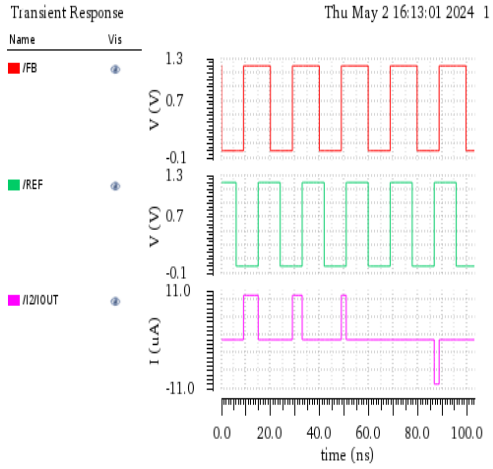

Figure 14. Output Waveforms of Charge Pump

reference signal (REF) while keeping the delay of feedback (FB) signal zero. Both signals would have the same frequency so that the delay would represent phase error. The period is taken to be 20 for both signals. After that, the average current at each delay is plotted vs the delay. It is expected for the positive delay to have a positive current that enters the CHP to minimize VCO control voltage and decrease the frequency of the FB signal CP needs very careful design as it has many non-idealities that result in spurious. tones thus these non-idealities need to be minimized. One of these non-idealities is the current mismatch. A current mismatch means that the amount of charge delivered to the loop filter from the upper current source for a certain period is different from the amount of charge discharged from the loop filter into the lower current source at the same time. Figure 15 shows the input and output of the frequency divider. Visibly, the output pulses have half the frequency of the input pulses. In other words, here, the comparative analysis of different parameters is shown. The parameters such as the number of transistors used in the design of PLL, supply voltage, and operating frequency power consumed are used to implement PLL and are analyzed above. From the analysis, the proposed PLL design has a 14% decrease in the number of transistors with a reduced area and 1000 times less power consumption. So, the proposed PLL can be effectively used in low-power digital electronic applications and compact devices. In the case of fractional-N frequency synthesizers, the VCO output is divided by a fractional value, as Fout = (N.F) x Fref[2]allowing the reference frequency to be larger, thus increasing the loop bandwidth and decreasing the values of N without affecting the frequency resolution the frequency resolution can be very high now as it is a fractional value of the reference frequency. Decreasing the value of N leads to a decrease in phase noise. as shown below in Figure 15

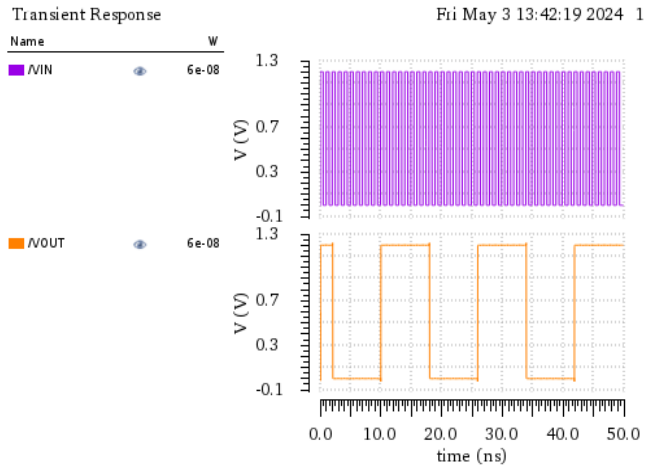

Figure 15. Output waveforms of Frequency Divider

Your final output waveform should resemble Figure 15 Notice that each half-wave of the output pulse comprises four half-pulses of the input, meaning the period of the output pulse is one-eighth of the input pulse period. Thus, our divider is functioning properly in that it divides. the input pulse frequency by 8

Table .1: shows the comparative analysis of the proposed design with previously reported structures. The parameters such as the number of transistors used. in the design of PLL, supply voltage, and operating frequency power consumed are used to implement PLL and are analyzed above. From the analysis, the proposed PLL

Table 1: Performance Summary and Comparison.

Parameters	***PLL [12]***	***This WORK [PLL]***
Technology	*90n*	*65n*
Number of transistors	*56*	*48*
Voltage	*1.8V*	*1.2V*
Operating frequency	*1GHZ*	*1GHZ*
Power Consumption	*4.2mW*	*194.24uW*
Total Power Consumed	*Medium*	*Low*
Frequency	*NA*	*5G*
I(cp)	*NA*	*10u A*

8. Future Work

The industry-wide trend is to move towards all-digital PLLs. Digital PLLs offer many advantages over analog PLLs mainly in the fact that. They eliminate the need for an analog loop filter as well as a charge pump, thereby saving area and power consumption [9].

9. Conclusions

A design of PLL using a cadence virtuoso tool in an analog design environment by using GPDK 65nm technology with a 1.2 V DC supply is performed. The simulation work presents a reduced number of transistors with a reduced area in the proposed design with very low power consumed at a DC voltage of 1.2 V. The Total Power Consumed by the proposed PLL design is 194.24 microwatts. We know that the power consumed, the sizing of the transistors, and the selection of the power supply voltage at different levels may vary with the total power consumed, respectively. This not only allows the working of PLL at high speed but also supports working at low power, which makes it very effective for low-power applications.

10. Acknowledgment

The Authors acknowledge the support of American University (AUC) who provided us with software tools for the preparation of our research study (CAD tools)

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